YM3439

Software-Controlled Sound Generator (SSGC)

■ OUTLINE

YM3439 (SSGC) is a sound source LSI that controlled by micro-processor. This LSI incorporates three square-wave generators, one noise generator and a envelope generator, which enables melody and effect sound generation. The LSI is made by CMOS process, and is compatible with YM2149 (SSG).

■ FEATURES

- Low power consumption of CMOS process.
- Register compatible with YM2149 (SSG).
- Sound source with three square-wave generators and one noise generator.
- 8-octave wide sound range.
- Smooth feeling sound decay is possible with 5-bit envelope generator.
- Built-in 3-channel 5-bit DAC.
- CPU parallel interface using 8-bit data bus.
- Built-in 2 channel 8-bit I/O ports enables interface with external systems.
- 5V single power supply.
- 40 pin plastic DIP or 44 pin plastic QFP.

YAMAHA CORPORATION

YM3439 CATALOG
CATALOG No. : LSI-2134392
1991. 06

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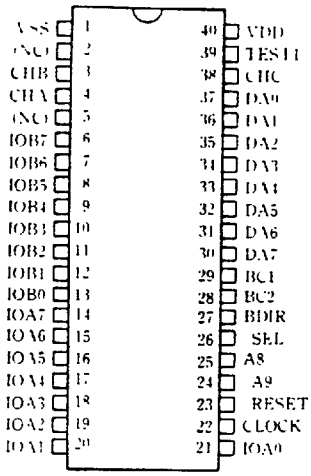
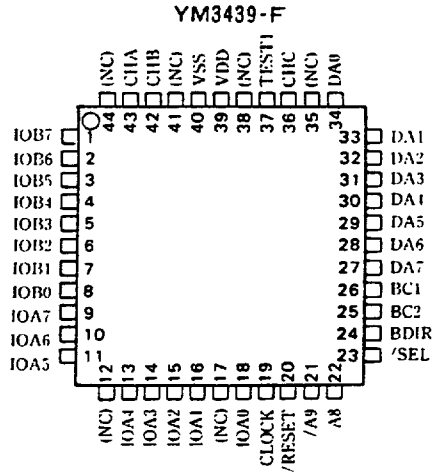
■ PIN CONFIGURATION

YM3439-D



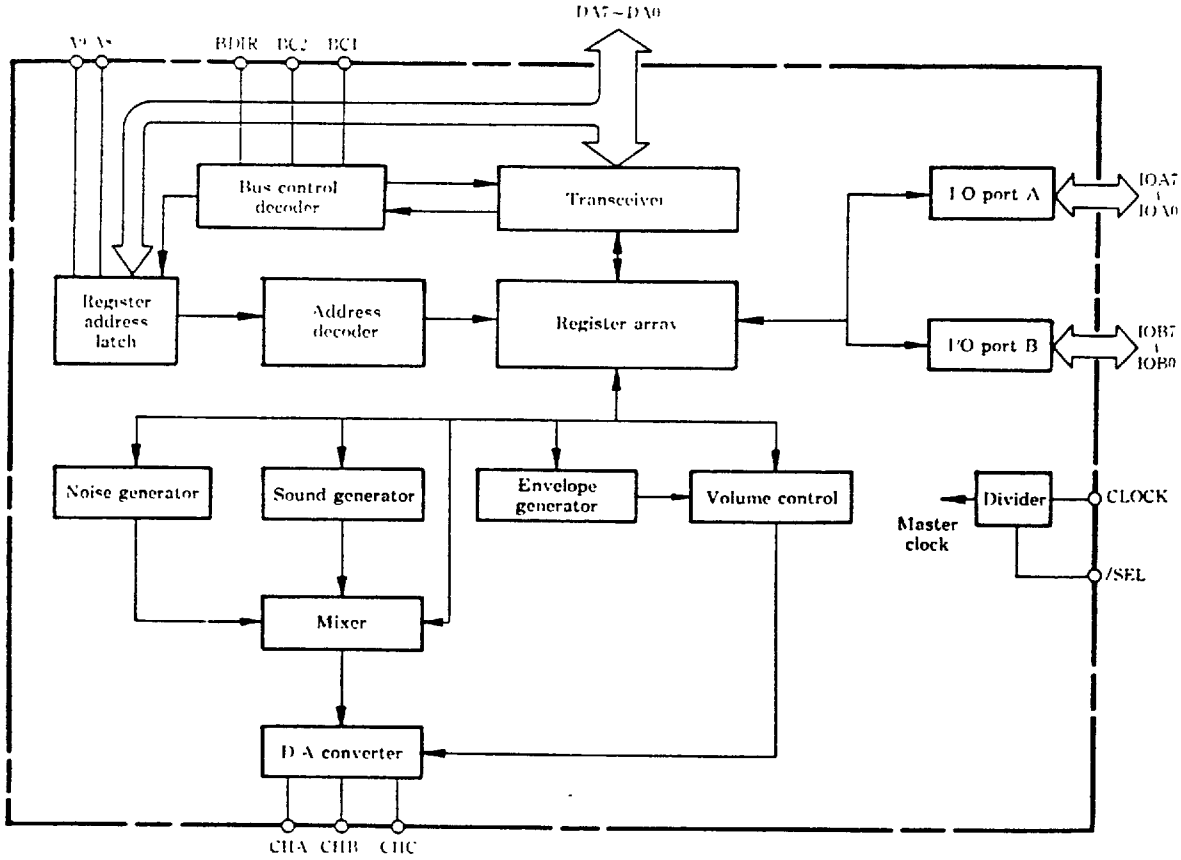
(40DIP Top View)

YM3439-F



(44QFP Top View)

■ BLOCK DIAGRAM



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■ PIN DESCRIPTION

Pin name	I/O	Function
VSS		Ground
CHB	O	CHANNEL B DAC OUTPUT
CHA	O	CHANNEL A DAC OUTPUT
IOB7	I+/O	I/O PORT B MSB
IOB6	I+/O	I/O PORT B bit6
IOB5	I+/O	I/O PORT B bit5
IOB4	I+/O	I/O PORT B bit4
IOB3	I+/O	I/O PORT B bit3
IOB2	I+/O	I/O PORT B bit2
IOB1	I+/O	I/O PORT B bit1
IOB0	I+/O	I/O PORT B LSB
IOA7	I+/O	I/O PORT A MSB
IOA6	I+/O	I/O PORT A bit6
IOA5	I+/O	I/O PORT A bit5
IOA4	I+/O	I/O PORT A bit4
IOA3	I+/O	I/O PORT A bit3
IOA2	I+/O	I/O PORT A bit2
IOA1	I+/O	I/O PORT A bit1
IOA0	I+/O	I/O PORT A LSB
CLOCK	I	Clock input for master clock
/RESET	I+	Reset input (low active)
/A9	I−	CPU interface address input
A8	I+	CPU interface address input
SEL	I+	Master clock setting ('L'; CLOCK/2, 'H'; CLOCK)
BDIR	I	CPU interface data bus control input
BC2	I	CPU interface data bus control input
BC1	I	CPU interface data bus control input
DA7	I/O	CPU interface data bus (MSB)
DA6	I/O	CPU interface data bus
DA5	I/O	CPU interface data bus
DA4	I/O	CPU interface data bus
DA3	I/O	CPU interface data bus
DA2	I/O	CPU interface data bus
DA1	I/O	CPU interface data bus
DA0	I/O	CPU interface data bus (LSB)
CHC	O	CHANNEL C DAC output
TEST1	O	LSI test terminal (Normally disconnected)
VDD		+5V power supply

Note) I+; input terminal with pulled-up resistor
I−; input terminal with pulled-down resistor

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■ FUNCTION DESCRIPTION

All functions of this LSI are controlled by 16 built-in registers. The CPU only writes data to these registers. upon which the LSI generates sound. The sound is generated by the following blocks.

- Sound generator: This generates a square wave with different frequencies for each channel (A, B and C).
- Noise generator: This generates a pseudo-random wave. (Frequency is variable.)
- Mixer: This mixes the sound and noise output of each channel (A, B and C).
- Sound volume control: This provides constant sound volume and variable sound volume for each channel (A, B and C). The constant sound volume is controlled by the CPU and the variable sound volume is controlled by the envelope generator.
- Envelope generator: This generates various envelopes (Single decay, repeat decay, etc.)
- D/A converter: The output level is determined by the sound volume control of each channel (A, B and C).

The CPU can read the register contents without affecting the sound.

1. CPU interface

Bi-directional data bus control of DA0 to DA7 of this LSI is carried out by the terminals; BDIR, BC1 and BC2.

CPU interface is set to the following modes depending on the settings of each terminal; BDIR, BC1 and BC2.

BDIR	BC2	BC1	Mode
L	L	L	Inactive mode
L	L	H	Address mode
L	H	L	Inactive mode
L	H	H	Data read mode
H	L	L	Address mode
H	L	H	Inactive mode
H	H	L	Data write mode
H	H	H	Address mode

Note) All modes can be set by fixing BC2 to "H" because bus control is redundant.

(1) Inactive mode

DA7 to DA0 terminals become high-impedance.

(2) Address mode

This mode reads the register address to be set.

DA7 to DA0 terminals become input terminals.

DA7 to DA0 are used together with A9 and A8 for address designation.

Upper address (Chip select)						Lower address			
/A9	A8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
L	H	L	L	L	L	Register address			

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The lower addresses DA3 to DA0 are used as a 16 register address.
The upper address works as chip select and DA3 to DA0 are read as register address only when /A9 and A8 are 'L' and 'H' respectively and DA7 to DA4 are 'L'. The register address which are read once will be held internally until the next address are read.

(3) Data write mode

This mode writes data to the addressed register.
DA7 to DA0 become data input terminals.

(4) Data read mode

This mode reads data from the addressed register.
DA7 to DA0 become data output terminals.

2. Register setting

The contents of the register array are shown below.

Register address	Name	Contents	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
0	R_0	Channel A frequency	8-bit fine tone adjustment							
1	R_1		×	×	×	×	4-bit rough tone adjustment			
2	R_2	Channel B frequency	8-bit fine tone adjustment							
3	R_3		×	×	×	×	4-bit rough tone adjustment			
4	R_4	Channel C frequency	8-bit fine tone adjustment							
5	R_5		×	×	×	×	4-bit rough tone adjustment			
6	R_6	Noise frequency	×	×	×	5-bit noise frequency				
7	R_7	I/O port and mixer setting	I/O		Noise			Tone		
			IOB	IOA	C	B	A	C	B	A
8	R_8	Channel A sound volume	×	×	×	M	L_3	L_2	L_1	L_0
9	R_9	Channel B sound volume	×	×	×	M	L_3	L_2	L_1	L_0
A	R_A	Channel C sound volume	×	×	×	M	L_3	L_2	L_1	L_0
B	R_B	Envelope frequency	8-bit fine adjustment							
C	R_C		8-bit rough adjustment							
D	R_D	Envelope shape	×	×	×	×	CONT	ATT	ALT	HOLD
E	R_E	I/O port A data	8-bit data							
F	R_F	I/O port B data	8-bit data							

Note) ×; don't care.

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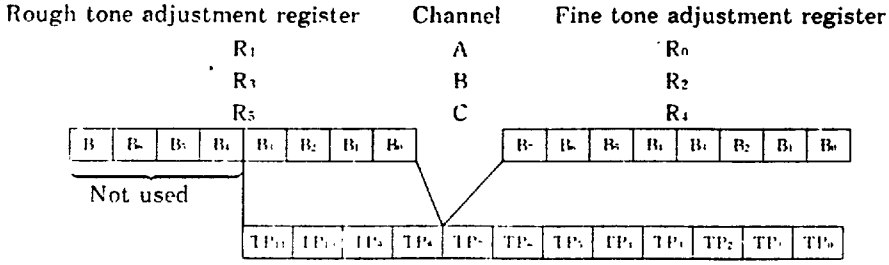
(1) Sound frequency setting (Controlled by registers R0 to R5)

The frequency of the square wave generated by the 3-channel (A, B and C) sound generator is set by the registers R0 to R5. R0 and R1 control channel A; R2 and R3 control channel B; and R4 and R5 control channel C respectively. Oscillating frequency f_1 is determined as follows from the set value TP.

$$f_1 = \frac{f_M}{16TP}$$

f_M refers to the master clock frequency.

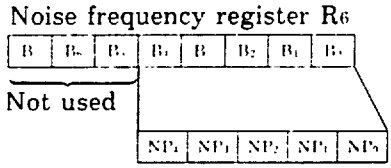


Set value of the 12-bit oscillating frequency (TP)

(2) Noise frequency setting (Controlled by register R6)

Noise frequency f_N is determined as follows from the set value NP.

$$f_N = \frac{f_M}{16NP}$$ (f_M is the master clock frequency)

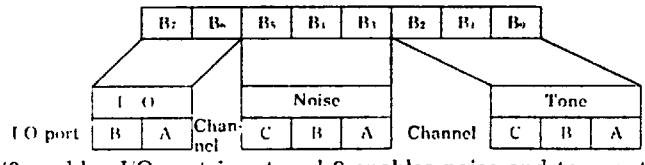


5-bit noise frequency set value (NP)

(3) Mixer, I/O port setting (Controlled by register R7)

The mixer mixes sound and noise. B5 to B0 of R7 determine the mixing sources. Sound with 0 written to the register will be output. Therefore, if 0 is written for both noise and sound, the mixed product will be output, and if 0 is written to only one of them, only the one with 0 will be output. If 1 is written to both, nothing will be output. Input and output of the I/O port is determined by B7 and B6 of R7. If 0 is written to the register, it denotes input.

I/O port and mixer setting register R7



(0 enables I/O port input and 0 enables noise and tone output.)

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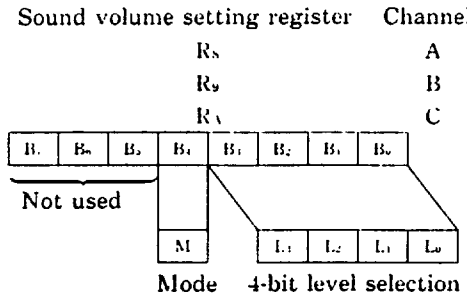
(4) Sound volume control (Controlled by R_8 to R_A)

The 3-channel (A, B and C) sound volume is controlled by the registers R_8 to R_A.

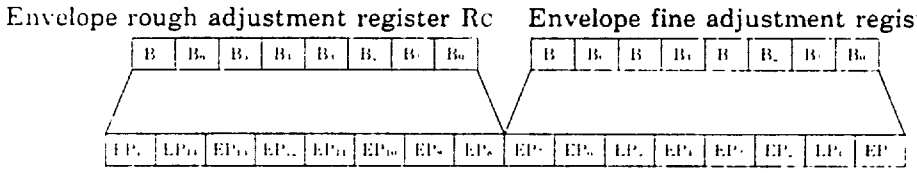


Mode M selects whether the fixed sound volume (M=0) or the variable sound volume (M=1) is set. When M=0, it selects one of 16 levels (4-bit level select signal L_3, L_2, L_1 and L_0) and generates sounds. L_3, L_2, L_1 and L_0 can be changed to change the sound volume. When M=1, the sound volume is determined by a 5-bit signal generated by the built-in envelope generator, and sound is generated.

(5) Envelope frequency setting (Controlled by R_B and R_C)

The envelope repeat frequency f_E is determined as follows from the envelope cycle set value EP:

$$f_E = \frac{f_M}{256EP}$$ (f_M is the master clock frequency)

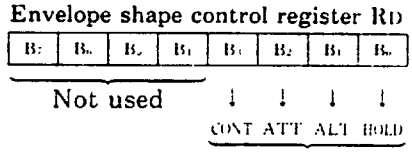


16-bit envelope cycle set value (EP)

The actual cycle of the frequency f_{EA} used with the envelope generator is 1/32 of the envelope repeat cycle ($1/f_E$).

(6) Envelope shape control (controlled by register R_D)

The envelope generator counts the envelope frequency f_{EA} 32 times per cycle of the envelope pattern. The envelope level is determined by this 5-bit counter output. The envelope shape is determined by increasing or decreasing this counter value, or stopping or repeating after one cycle. The shape is controlled by the registers B_3 to B_0 of R_D.



Envelope shape control signal

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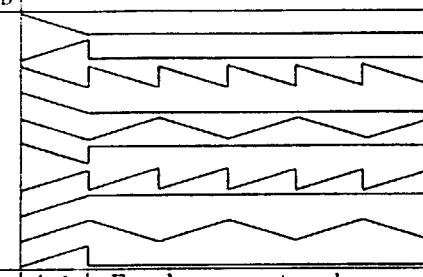
The envelope can be shaped in various ways as shown in table 4 by CONT, ATT, ALT and HOLD.

B_3 CONT	B_2 ATT	B_1 ALT	B_0 HOLD	Envelope shape
0	0	×	×	
0	1	×	×	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	



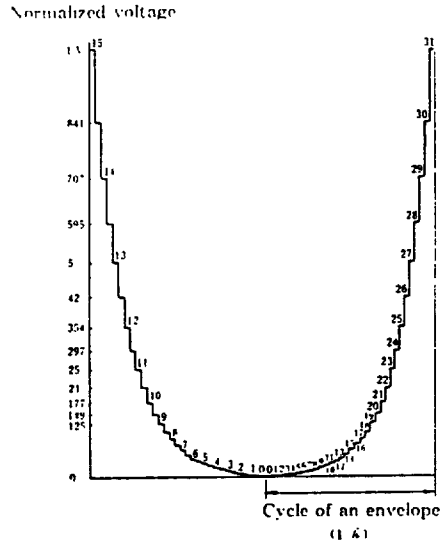
$1/f_r$ Envelope repeat cycle

(7) I/O port (Register R_E and R_F)

Registers R_E and R_F are used for storage of data that is to be written from the CPU into the I/O. R_E is the register for IOA and R_F is for IOB.

3. D/A converter

The D/A converter converts to the following outputs when the maximum amplitude is normalized to 1V. This is a linear logarithmic conversion, which has wide dynamic range and gives a natural feeling decay to the sound.



D/A converter output level

(Notes)

The numbers on the left half of the figure are the fixed sound volume select signals; L_3, L_2, L_1 and L_0 in decimals and the numbers in the right half is envelope counter output in decimals.

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■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.5 ~ 7.0	V
Input voltage	V_I	−0.5 ~ V_{DD}+0.5	V
Operating temperature	T_{OP}	0 ~ 70	°C
Storage temperature	Tstg	−50 ~ 125	°C

2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	T_{OP}	0	25	70	°C

3. DC Characteristics (Conditions; Ta=0 ~ 70°C, V_{DD}=5.0 ± 0.25V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power consumption	W	V_{DD}=5.0V, *1		8.0	10.0	mW
Input voltage H level	V_{IH}	*2	2.2			V
Input voltage L level	V_{IL}	*2			0.8	V
Input pulled-up resistance	R_U	*3	60		600	KΩ
Input pulled-down resistance	R_D	Applied to /A9	60		600	KΩ
Input leakage current	I_{LI}	*4	−10		10	μA
Output voltage H level	V_{OH}	I_{OH}=100μA, *5	2.5			V
Output voltage L level	V_{OL}	I_{OL}=1.6 mA, *5			0.4	V
Output leakage current	I_{LO}	*6	−10		10	μA
Analog maximum output voltage	V_{OA}	R_L=1KΩ, *7	0.96	1.00	1.35	Vpp

*1) When /SEL='H' and fc=2MHz.

*2) Applied to all input terminals. Applied to the terminals; IOA7 to IOA0, IOB7 to IOB0 and DA7 to DA0 during input mode.

*3) Applied to the terminals: /RESET, /SEL and A8. Applied to the terminals; IOA7 to IOA0 and IOB7 to IOB0 during input mode.

*4) Applied to the terminals: CLOCK, DBIR, BC1 and BC2. Applied to the terminals DA7 to DA0 during input mode.

*5) Applied to the output terminals except for CHA, CHB and CHC. Applied to the terminals IOA7 to IOA0, IOB7 to IOB0 and DA7 to DA0 during the output mode.

*6) Applied to DA7 to DA0 during high impedance.

*7) Applied to CHA, CHB and CHC.

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4. AC Characteristics (Conditions: Ta=0 ~ 70°C, V_{DD}=5.0 ± 0.25V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
CLOCK	Frequency *1	fc	1.0		4.0	MHz
	Rise time	tr			50	ns
	Fall time	tf			50	ns
	Duty		40	50	60	%
BDIR, BC1 and BC2 transit time		tBD			30	ns
/RESET Reset pulse width		tRW	500			ns
Reset - Bus control						
	Wait time	tRB	100			ns
Address mode						
	Setup time	tAS	300			ns
	Hold time	tAH	80			ns
Data write mode						
	Write time	tDW	0.3		10	μs
	Setup time	tDS	0			μs
	Hold time	tDH	80			μs
Data read mode						
	Access time	tDA			400	μs
High impedance delay time		tDF			100	μs

*1) Max. 2MHz when /SEL=H.

5. Timing Chart

Fig. 1 Clock timing

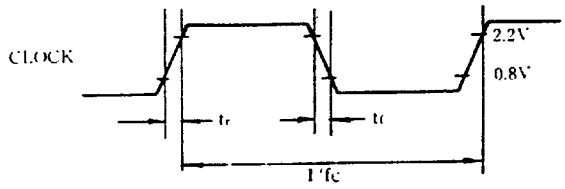

Fig. 2 Bus control timing

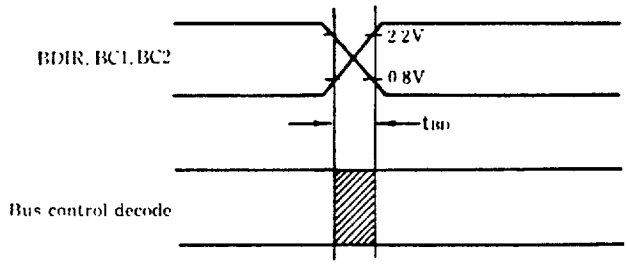

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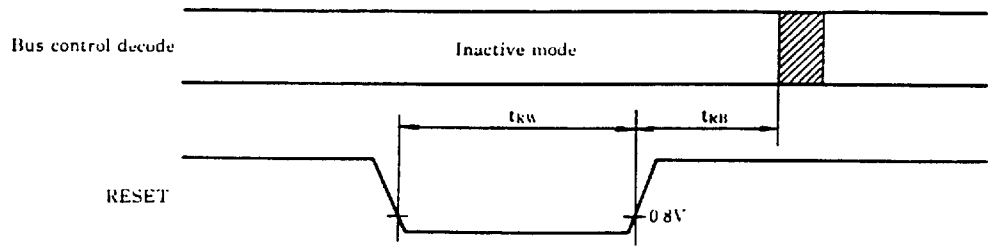
Fig. 3 Reset timing



Note) Must carry out reset in inactive mode.
The time TRB is needed until the mode is changed after reset.

Fig. 4 Address mode timing

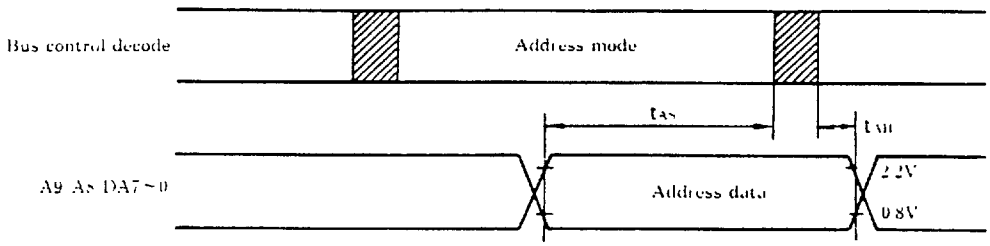


Fig. 5 Data write mode timing

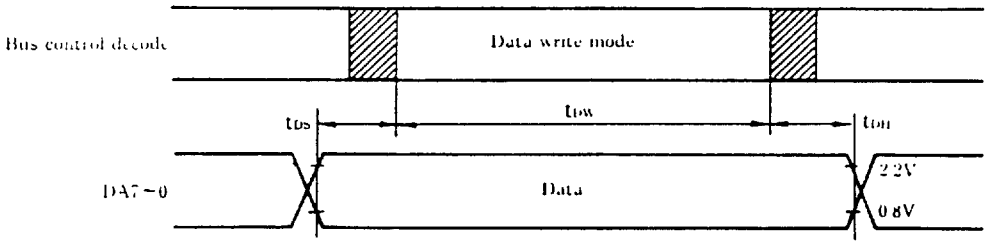
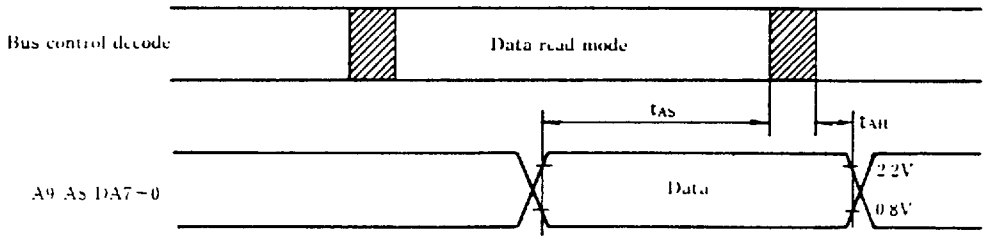


Fig. 6 Data read mode timing



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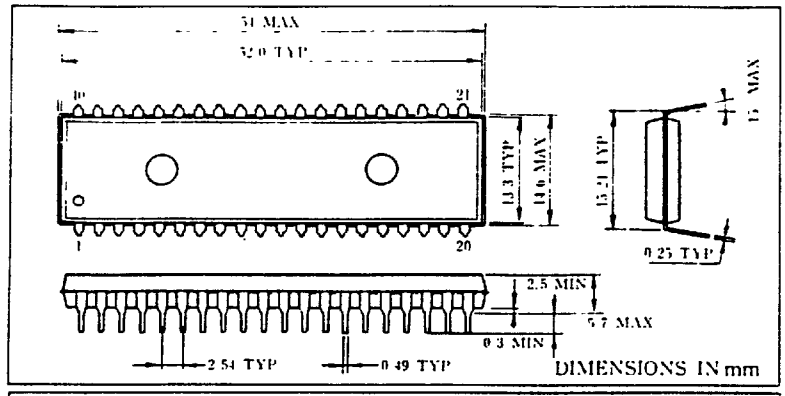
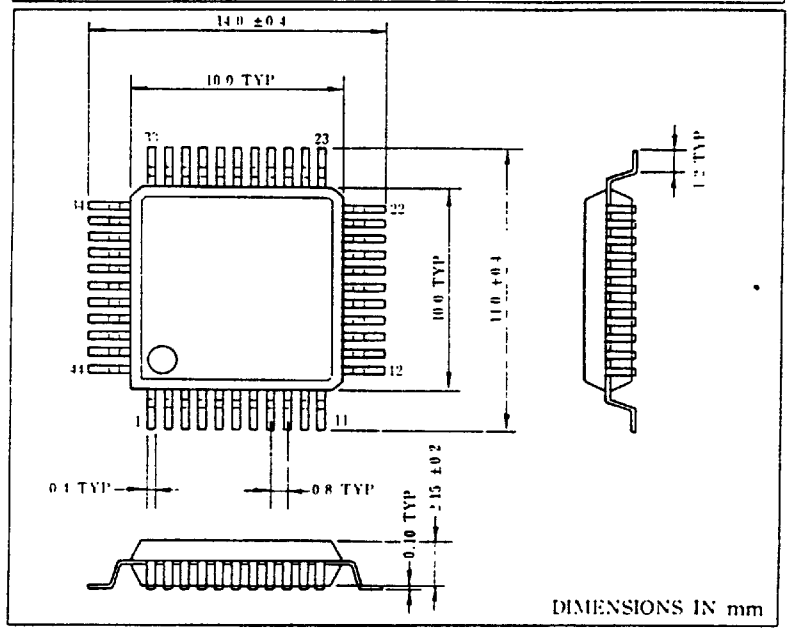
■ EXTERNAL DIMENSIONS

(1) YM3439-D



(2) YM3439-F



The specifications of this product are subject to improvement changes without prior notice.

AGENCY

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